LSI Design Verification Using Topology Extraction

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ABSTRACT

A system for design verification of LSI components using programs which convert artwork to circuit and logic schematics (topology extraction) is discussed. Algorithms are described, limitations are discussed, and results are presented.

I) INTRODUCTION

A major problem associated with VLSI is the length of the design cycle. It may take as much as three years for a design to progress from conception to production. Computer Aided Design tools play a major role in the attempt to reduce this design cycle. A verification tool, for example, attempts to reduce the amount of debugging time required by verifying that a design is correct before it is built. Such a tool is particularly useful after those design stages which require manual intervention, for then the verifier will provide reassurance that the manual steps were performed correctly. For example, a logic simulator may be used to verify that the logic design is correct.

Efficient auto-layout tools are not yet available. The alternative, manual mask layout, is a major design step which can introduce numerous errors. The programs presented in this paper aid in verifying the electrical connectivity, circuit level functionality and logic level functionality of the mask layout.

II) OBJECTIVES

The objective of the design verification programs is to verify that the function as implemented in the artwork is the same as the desired function described by the designer. Verification is attempted on two different levels of detail: the component level and the logic gate level. On either level, the verification may be attempted two different ways: simulation or direct comparison.

Simulation - The circuit description extracted from the artwork is simulated at the transistor or logic gate level using a known set of vectors. This result is compared with the results of the earlier design phase simulations. In this case the verification is only as good as the effectiveness of the test vectors at exercising the designed function. Because the artwork and test vectors are normally kept in machine readable format this test requires no additional effort from the designer.

Direct Comparison - The description extracted from the artwork is directly compared with the intended schematic. This requires that the intended schematic be in a machine readable format. The advantage of this method is that it will remain viable as chips increase in complexity, provided that the artwork is hierarchically structured. In such a case, the comparison can be applied cell by cell on all levels of the hierarchy. The main disadvantage of this method is that it depends on the correctness of the original schematic. An incorrect design which is implemented correctly will still pass this test. If some method is available for assuring the correctness of the original schematic, however, then this flaw can be corrected.

III) AN OVERVIEW OF EXTRACTION

Topology extraction is the process of directly translating the artwork into a table of nodes and interconnecting transistors, and then into a logic gate description. The process also extracts certain parameters affecting circuit performance. The description, generated by the process, must be suitable for satisfying the objectives defined in the previous section.

The topology extraction system is composed of two phases. In the first phase, the transistor level description is extracted from the artwork. Using information about expected device topologies, the system can identify devices in the artwork, and compute their parameters. The system then computes parasitic capacitance for each node. Similiar systems have been reported in the literature.[1-4]

In the second phase, the logic gate description is extracted, along with the associated propagation delays. This phase identifies the topology of logic gates: and-or-invert, or-and-invert, PLA, and others. Gate propagation delays are estimated from transistor parameters and node capacitances.

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